In the Claims:

1. (Original) A ferroelectric memory device, comprising:

a semiconductor substrate having a transistor;

a first interlayer dielectric on the semiconductor substrate;

a plug penetrating the first interlayer dielectric;

a capacitor electrically connected to the plug, the capacitor having a bottom electrode that has a top surface and a plurality of side surfaces, a capacitor-ferroelectric layer and a top electrode; and

a reaction buffer layer between the first interlayer dielectric and the capacitor-ferroelectric layer.

2. (Original) The ferroelectric memory device of Claim 1, wherein the reaction buffer layer is adjacent to the side surfaces of the bottom electrode, and wherein a top surface of the reaction buffer layer and the top surface of the bottom electrode form a planar surface.

3. (Original) The ferroelectric memory device of Claim 2, further comprising a third interlayer dielectric under the reaction buffer layer, and wherein the reaction buffer layer comprises a material that prevents a reaction between the third interlayer dielectric and the capacitor-ferroelectric layer.

4. (Original) The ferroelectric memory device of Claim 2, wherein the reaction buffer layer is formed of a material selected from the group consisting of titanium oxide, tantalum oxide and aluminum oxide.

5. (Original) The ferroelectric memory device of Claim 2, further comprising:

a bit line that is electrically connected to the transistor on the first interlayer dielectric; and

a third interlayer dielectric recessed between the bottom electrode and a second bottom electrode associated with a capacitor of an adjacent ferroelectric memory device.

6. (Original) The ferroelectric memory device of Claim 5, wherein the reaction buffer layer is on the third interlayer dielectric.

7. (Original) The ferroelectric memory device of Claim 5, further comprising a second interlayer dielectric between the first interlayer dielectric and the third interlayer dielectric, wherein the plug further penetrates the second interlayer dielectric to electrically connect the bottom electrode to the semiconductor substrate.

8. (Original) The ferroelectric memory device of Claim 1, further comprising a first diffusion barrier on the first interlayer dielectric and side surfaces of the bottom electrode.

9. (Original) The ferroelectric memory device of Claim 8, wherein the first diffusion barrier comprises an oxygen diffusion barrier.

10. (Original) The ferroelectric memory device of Claim 1, wherein the bottom electrode comprises:

a first material that serves as an oxygen diffusion barrier;

a second material for providing the capacitor-ferroelectric layer with oxygen on the first material; and

a third material having a lattice point that allows for formation of a capacitor-ferroelectric layer having a crystalline structure.

11. (Original) The ferroelectric memory device of Claim 10, wherein the first material is iridium, the second material is iridium oxide, and the third material is platinum.

12. (Original) The ferroelectric memory device of Claim 1, wherein the top electrode comprises a fourth material for providing the capacitor-ferroelectric layer with oxygen and a fifth material that is selected to improve the strength of the fourth material.

13. (Original) The ferroelectric memory device of Claim 12, wherein the fourth material is on the capacitor-ferroelectric and the fifth material is on the fourth material.

14. (Original) The ferroelectric memory device of Claim 12, wherein the fourth material is iridium oxide, and the fifth material is iridium.

15. (Original) The ferroelectric memory device of Claim 12, further comprising a second diffusion barrier on the capacitor-ferroelectric layer and on the top electrode.

16. (Original) The ferroelectric memory device of Claim 15, wherein the second diffusion barrier acts as a hydrogen diffusion barrier.

17. (Original) The ferroelectric memory device of Claim 16, wherein the second diffusion barrier comprises an aluminum oxide layer.

18. (Original) The ferroelectric memory device of Claim 1, further comprising:
a fourth interlayer dielectric on the top electrode;
a first metal line on a part of the fourth interlayer dielectric;
a fifth interlayer dielectric on the fourth interlayer dielectric;
a via hole that exposes the top surface of the top electrode; and
a second metal line in the via hole that is electrically connected to the top electrode.

19. (Original) The ferroelectric memory device of Claim 18, wherein the first metal line and the second metal line each comprise an aluminum metal line.

20. (Original) The ferroelectric memory device of Claim 5, further comprising a first contact pad between the bit line and the semiconductor substrate.

21. (Original) The ferroelectric memory device of Claim 20, wherein the first contact pad comprises a polysilicon contact pad.

22. (Original) The ferroelectric device of Claim 21, further comprising a second contact pad between the plug and the semiconductor substrate.

23. (Original) A ferroelectric memory device, comprising:

a semiconductor substrate having a transistor;

a first interlayer dielectric on the semiconductor substrate that surrounds a gate electrode of the transistor;

a capacitor on the first interlayer dielectric, the capacitor comprising:

a buried bottom electrode on the first interlayer dielectric, the bottom electrode having a top surface and a plurality of side surfaces;

a capacitor-ferroelectric layer on the buried bottom electrode; and

a top electrode on the capacitor-ferroelectric layer;

a planarizing layer adjacent to the side surfaces of the bottom electrode, wherein a top surface of the planarizing layer and the top surface of the bottom electrode form a planar surface and wherein the capacitor-ferroelectric layer is on the planar surface; and

a plug that penetrates the first interlayer dielectric under the bottom electrode, wherein the plug is electrically connected to the bottom electrode.

24. (Original) The ferroelectric memory device of Claim 23, wherein the planarizing layer comprises a reaction buffer layer.

25. (Original) The ferroelectric memory device of Claim 24, further comprising a third interlayer dielectric on the first interlayer dielectric and under the reaction buffer layer, wherein the reaction buffer layer comprises a material that prevents a reaction between the third interlayer dielectric and the capacitor-ferroelectric layer.

26. (Original) The ferroelectric memory device of Claim 25, wherein the reaction buffer layer is formed of a material selected from the group consisting of titanium oxide, tantalum oxide and aluminum oxide.

27. (Original) The ferroelectric memory device of Claim 24, wherein the bottom electrode comprises:

a first material that serves as an oxygen diffusion barrier;

a second material for providing the capacitor-ferroelectric layer with oxygen on the first material; and

a third material having a lattice point that allows for formation of a capacitor-ferroelectric layer having a crystalline structure.

28. (Original) The ferroelectric memory device of Claim 27, wherein the first material is iridium, the second material is iridium oxide, and the third material is platinum.

29. (Original) The ferroelectric memory device of Claim 24, wherein the top electrode comprises a fourth material for providing the capacitor-ferroelectric layer with oxygen and a fifth material that is selected to improve the strength of the fourth material.

30. (Original) The ferroelectric memory device of Claim 29, wherein the fourth material is iridium oxide, and the fifth material is iridium.

31-48. (Canceled).